

**What is claimed is:**

1.           A semiconductor memory device, comprising:  
            a semiconductor substrate; and  
            gate electrodes formed for a transistor on  
5   said semiconductor substrate through a gate insulating  
    film,  
            wherein a gate length of said gate electrode  
    is longer than a minimum processing dimension.
- 10   2.           The semiconductor memory device according to  
    claim 1, further comprising:  
            a first diffusion layer formed in a surface  
    of said semiconductor substrate to function as one of  
    a source and a drain; and  
15              a second diffusion layer formed in the  
    surface of said semiconductor substrate to function as  
    the other of said source and said drain,  
            wherein the shortest distance between said  
    first diffusion layer and said second diffusion layer  
20   is proportional to said gate length.
3.           The semiconductor memory device according to  
    claim 2, further comprising:  
            a gate insulating film formed on said  
25   semiconductor substrate and extending over said first  
    diffusion layer and said second diffusion layer,  
            wherein said gate electrode is formed on said

gate insulating film.

4. The semiconductor memory device according to claim 2, further comprising:

5 a first insulating film provided to cover said gate electrode;

a first contact section formed to pass through said first insulating film to said first diffusion layer;

10 a bit line formed on said insulating film;

a second contact section formed to pass through said insulating film to said second diffusion layer; and

a capacitive section formed on said first  
15 insulating film and connected to said first contact section.

5. The semiconductor memory device according to claim 4, wherein a side length or diameter of said  
20 first contact section is said minimum processing dimension; and

a side length or diameter said second contact section is said minimum processing dimension.

25 6. The semiconductor memory device according to claim 5, further comprising:

a second insulating film formed to cover said

first insulating film, said first contact section,  
said second contact section and said bit line;

wherein said capacitive section is formed on  
said second insulating film, and said capacitive  
5 section comprises a lower electrode, a capacitive  
insulating film formed on said lower electrode and an  
upper electrode formed on said capacitive insulating  
film; and

a third contact section formed to pass  
10 through said second insulating film to said first  
contact section.

7. The semiconductor memory device according to  
claim 1, wherein an impurity concentration of said  
15 semiconductor substrate is lower than an impurity  
concentration of said semiconductor substrate when the  
gate length of said gate electrode is said minimum  
processing dimension.

20 8. The semiconductor memory device according to  
claim 1, wherein the gate length of said gate  
electrode is equal to or longer than 1.3 times said  
minimum processing dimension.

25 9. A semiconductor memory device, comprising:  
a first MOS transistor formed on a first  
surface of a semiconductor substrate; and

a second MOS transistor formed on a second surface of said semiconductor substrate,

wherein said first MOS transistor has a first gate electrode,

5           said second MOS transistor has a second gate electrode, and

a gate length of said first gate electrode and a gate length of said second gate electrode are longer than a minimum processing dimension.

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10.       The semiconductor memory device according to claim 9, wherein said first MOS transistor further comprises a first diffusion layer functioning as one of a source and a drain and a second diffusion layer  
15       functioning as the other of said source and said drain,

          said second MOS transistor further comprises a third diffusion layer functioning as one of said source and said drain and said second diffusion layer  
20       functioning as the other of said source and said drain,

          said second diffusion layer is used in common to said first MOS transistor and said second MOS transistor,

25       the shortest distance between said first diffusion layer and said second diffusion layer is proportional to the gate length of said first gate

electrode, and

the shortest distance between said third diffusion layer and said second diffusion layer is proportional to the gate length of said second gate electrode.

11. The semiconductor memory device according to claim 10, wherein said first MOS transistor further comprises a first gate insulating film extending over said first diffusion layer and said second diffusion layer,

said second MOS transistor further comprises a second gate insulating film extending over said third diffusion layer and said second diffusion layer, said first gate electrode is formed on said first gate insulating film, and

said second gate electrode is formed on said first gate insulating film.

12. The semiconductor memory device according to claim 10, further comprising:

a first insulating film formed to cover said first gate electrode and said second gate electrode;

a first contact section formed to pass through said first insulating film to said first diffusion layer;

a bit line formed on said first insulating

film;

a second contact section formed to pass through said first insulating film to said second diffusion layer;

5 a third contact section formed to pass through said first insulating film to said third diffusion layer;

a first capacitive section formed on said first insulating film and connected to said first  
10 contact section; and

a second capacitive section formed on said first insulating film and connected to said third contact section.

15 13. The semiconductor memory device according to claim 12, wherein a side length or diameter of said first contact section is said minimum processing dimension,

a side length or diameter of said second  
20 contact section is said minimum processing dimension, and

a side length or diameter of said third contact section is said minimum processing dimension.

25 14. The semiconductor memory device according to claim 13, further comprising:

a second insulating film formed to cover said

first insulating film, said first contact section, said second contact section, said third contact section and said bit line;

wherein said first capacitive section and  
5 said second capacitive section are formed on said second insulating film, and each of said first capacitive section and said second capacitive section has a lower electrode, a capacitive insulating film formed on said lower electrode and an upper electrode  
10 formed on said capacitive insulating film; and

a fourth contact section formed to pass through said second insulating film to said first contact section; and

a fifth contact section formed to pass  
15 through said second insulating film to said third contact section.

15. The semiconductor memory device according to claim 9, wherein a gate interval between said first  
20 gate electrode and said second gate electrode is said minimum processing dimension.

16. The semiconductor memory device according to claim 9, wherein an impurity concentration of said  
25 semiconductor substrate is lower than an impurity concentration of said semiconductor substrate when the gate length of said first gate electrode and the gate

length of said second gate electrode are said minimum processing dimension.

17.       The semiconductor memory device according to  
5 claim 9, wherein the gate length of said first gate  
electrode and the gate length of said second gate  
electrode are equal to or longer than 1.3 times said  
minimum processing dimension.